CLAIMS

1. A parallel data bus comprising:
   a) at least one channel for data, said data being characterized by a bit time; and
   b) a clocking and control channel for clock synchronization and data control information, said clocking and control channel carrying a signal, said signal having high and low times in units equal to one said bit time.

2. A parallel data bus as recited in claim 1, wherein said signal has first and second edges, said first edge having fixed phase and said second edge being phase-modulated.

3. A parallel data bus as recited in claim 1, said clocking and control channel having a clock rate and said parallel data bus carrying data multiplexed at a multiplexing cycle rate, wherein said clock rate is chosen to be equal to said multiplexing cycle rate.

4. A parallel data bus as recited in claim 2, wherein said first edge carries bit timing information for said clock synchronization.

5. A parallel data bus as recited in claim 2, wherein said second edge carries at least control data information.

6. A parallel data bus as recited in claim 2, wherein said second edge carries at least framing data.

7. A parallel data bus as recited in claim 2, wherein said second edge carries control data information and framing data.

8. A parallel data bus as recited in claim 4, wherein said first edge regulates a delay-locked loop for extending said clock synchronization.

9. A parallel data bus as recited in claim 4, wherein said first edge regulates a phase-locked loop for extending said

clock synchronization.

10. A parallel data bus comprising:

a) at least one channel for data, said data being characterized by a bit time; and

b) a clocking and control channel for clock synchronization and data control information, said clocking and control channel carrying a signal, said signal having high and low times in units equal to one said bit time and said signal having first and second edges, said first edge having fixed phase for carrying bit timing information for said clock synchronization, and said second edge being phase-modulated for carrying at least said data control information.

11. A parallel data bus as recited in claim 10, said clocking and control channel having a clock rate and said parallel data bus carrying data multiplexed at a multiplexing cycle rate, wherein said clock rate is chosen to be equal to said multiplexing cycle rate.

12. A parallel data bus as recited in claim 10, wherein said second edge carries control data information and framing data.

13. A parallel data bus as recited in claim 10, wherein said first edge regulates a delay-locked loop for extending said clock synchronization.

14 A parallel data bus as recited in claim 10, wherein said first edge regulates a phase-locked loop for extending said clock synchronization.